Notice of References Cited Application/Control No. Applicant(s)/Patent Under Reexamination KLEIN, ROBERT C. Examiner Art Unit Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-6,742,170 B2	05-2004	Elzinga et al.	716/10
	В	US-6,202,194 B1	03-2001	Seningen et al.	716/10
	С	US-2003/0177450 A1	09-2003	Nugent	716/1
	D	US-2002/0144227 A1	10-2002	Das et al.	716/12
	Е	US-6,597,362 B1	07-2003	Norman	345/505
	F	US-6,014,509 A	01-2000	Furtek et al.	716/16
	G	US-6,083,274 A	07-2000	ladonato et al.	716/10
	Н	US-6,815,621 B2	11-2004	Park et al.	174/260
	1	US-6,725,442 B1	04-2004	Cote et al.	716/16
	J	US-			
	к	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	Z					
	0					
	բ					
	σ					
	R					
	s					
	Т					

NON-PATENT DOCUMENTS

	HON-I ATEM DOCUMENTS				
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Chen, Hongyu "Physical Planning of on-Chip Interconnect Architectures", IEEE International Conference on Computer Design: VLSI in Computers and Processors, 16 - 18 Sept. 2002, pp. 30 - 35			
	٧				
	w				
	х				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYYY format are publication dates. Classifications may be US or foreign.